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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/856,209	05/18/2001	Kozo Nakamura	82822	6736

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WELSH & KATZ, LTD
120 S RIVERSIDE PLAZA
22ND FLOOR
CHICAGO, IL 60606

EXAMINER	
SONG, MATTHEW J	

ART UNIT	PAPER NUMBER
1765	

DATE MAILED: 07/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/856,209	NAKAMURA ET AL.	
	Examiner	Art Unit	
	Matthew J Song	1765	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17 and 18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/3/2004 has been entered.

Claim Objections

2. Claims 17 and 18 recites the limitation "cutting the wafers" in line 10. There is insufficient antecedent basis for this limitation in the claim, likewise for claim 18.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 17-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Iida et al (US 5,968,264).

In a method of manufacturing a crystal ingot, note entire reference, Iida teaches a silicon single crystal grown through the use of a crystal pulling apparatus, where wafers were sliced

from the thus-obtained silicon ingot (col 14, ln 20-67). Iida also teaches (Delta G=G_e-G_c) is not greater than 5°C/cm, where G_e is a temperature gradient at the periphery and G_c is a temperature gradient at the center portion of a growing crystal (col 10, ln 5-15). Iida also teaches a G_c=30°C/cm (3.0 °C/mm) and a G_e=35°C/cm (3.5 °C/mm)(Fig 8), where the G_e/G_c ratio can be determined to be 1.16. Iida also discloses that wafers were sliced from the thus-obtained silicon ingot (col 14, ln 20-67) Iida also teaches an OSF region is observed between a N region, a neutral region having few defects, and a vacancy rich region and interstitial rich region (col 15, ln 1-15 and Fig 10A). Iida also teaches the G_c is the temperature gradient at a central portion of the growing crystal both in an in-crystal descending zone, 1300-100°C, or in the vicinity of the solid-liquid interface of the crystal, melting point of silicon to 1400°C (col 4, ln 5-15 and col 4, ln 35-39), therefore G_c reads on applicant's $G1_{center}$ and $G2_{center}$. The value of 1.06x ($G1_{center}$ and $G2_{center}$)$^{-0.2}$ can be determined to be 0.68. Iida also teaches an OSF ring with an inner diameter of at least ½ a wafer inner diameter (Fig 10A) at a pulling speed of 0.62 mm/min. Iida et al also discloses G_e is the temperature gradient at a peripheral portion of the crystal and G_c is a temperature gradient at a central portion, where both are in an in-crystal descending temperature zone between 1420°C and 1350°C or between a melting point of silicon and 1400°C in the vicinity of the solid-liquid interface (col 10, ln 1-15), this reads on applicants' temperature region from the solid-liquid interface temperature to approximately 1350°C.

Response to Arguments

5. Applicant's arguments filed 5/3/2004 have been fully considered but they are not persuasive.

Applicants' argument that Iida et al does not suggest a wafer having growth defects can be a wafer for semiconductor production is noted but is not found persuasive. Iida et al is directed to forming a defect-free wafer, as suggested by applicants, however Iida et al also teaches varying the pulling rate of a silicon single crystal during production between a high pulling rate and a low pulling rate to determine the optimal pulling rate while controlling the temperature gradient at the periphery and the center of the silicon crystal (Example 1 and Figure 8). By varying the pulling rate, as taught by Iida et al, and controlling the temperature gradient, a method of forming a silicon single crystal having a defect region is inherently taught, note Figures 10A and 10B. Iida et al does not teach a defect rich wafer is desirable, but Iida et al does teach a method of forming a vacancy rich wafer and forming a vacancy rich wafer is well known in the art to be desirable, note Park et al (US 6,472,040), below.

Applicants' arguments regarding the attached Figure A have not been considered because no attached Figure A is included with the instant remarks.

Applicants' argument that Iida et al does not suggest the range of $G1_{edge}/G1_{center}$ is noted but is not found persuasive. Iida et al teaches a $G1_{edge}/G1_{center}$ ratio of 3.5/3.0 (1.16) (Figure 8), which is within the claimed ranged; therefore anticipates the claimed range. Iida et al is not required to teach the range because Iida et al teaches a point within the claimed range; therefore the entire range is anticipated.

Applicants' argument that Iida et al does not teach the control parameters of the present invention is noted but is not found persuasive. Iida et al teaches controlling the temperature gradient at the edge and center to be 3.5 °C/mm and 3.0°C/mm, respectively, which is the primary control parameter claimed by applicants. Applicants also claimed an OSF ring

diameter/crystal diameter ratio of greater than 0.5, which is also taught by Iida et al. Iida et al teaches OSF ring diameter varies directly with pulling speed and an OSF ring/crystal diameter ratio of greater than 0.5 occurs at a pulling speed of approximately 0.65 mm/min, note Figure 10A.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Park et al (US 6,472,040) teaches pulling a silicon ingot to from a vacancy rich region (col 3, ln 35-45) and varying pulling rate between 1.2 mm/min and 0.4 mm/min to determine a preferred pulling rate (col 10, ln 10-25).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew J Song whose telephone number is 571-272-1468. The examiner can normally be reached on M-F 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nadine Norton can be reached on 571-272-1465. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew J Song
Examiner
Art Unit 1765

MJS

NADINE G NORTON
SUPERVISOR